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D1
a gray code counter using a gray code, responsive to an output of said detector, for selectively generating one of a signal to increase an amount of delay of said delay circuit and a signal to decrease said amount of delay of said delay circuit;

wherein said output of said detector indicates that said first clock is in advance of said second clock in a phase or said second clock is in advance of said first clock in a phase.

D2
11. (Three Times Amended) A semiconductor device comprising a delay locked loop including:

E1
a first input buffer receiving at least a first external clock and a second external clock complementary in phase to said first external clock, and outputting a first internal clock at the timing of the rising edge of said first external clock when a potential of said first external clock is equal to that of said second external clock;

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a second input buffer receiving at least said first and second external clocks, and outputting a second internal clock at the timing of the rising edge of said second external clock when a potential of said first external clock is equal to that of said second external clock;

a first delay circuit delaying said first internal clock to output a third internal clock;

a second delay circuit delaying said second internal clock to output a fourth internal clock;

a detector detecting which of said first and second clocks is advanced in a phase; and

a gray code counter using a gray code, responsive to an output of said detector, for selectively generating one of a signal to increase an amount of delay of said first delay circuit and an amount of delay of said second delay circuit, and a signal to decrease said amount of delay of said first delay circuit and said amount of delay of said second delay circuit;

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wherein said output of said detector indicates that said first clock is in advance of said second clock in a phase or said second clock is in advance of said first clock in a phase.
